In the Abstract

Amend the Abstract as follows:

~~Input and output boundary scan cells respectively include latchable input and output buffers (103,40) which respectively utilize the input and output buffers of the integrated circuit in which the boundary scan cells are provided. The latchable input and output buffers provide the input and output boundary scan cells with a low overhead latching function.~~ A process initializes the state of an output memory circuit of a scan cell located at the boundary of a logic circuit within an integrated circuit. Data is scanned into an input memory circuit of the cell while maintaining the cell in a mode providing normal operation of the logic circuit. The cell is placed in a test mode that disables normal operation of the logic circuit. The data scanned into the input memory circuit is transferred into the output memory circuit simultaneous with the placing the cell in the test mode. A transmission gate between the logic circuit and the output memory circuit and a transmission gate between the input memory circuit and the output memory circuit effect the changes between normal operation and test modes.